EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Sean A. Pryor (RN: 48,103) on February 26, 2009.

The application has been amended as follows:

IN THE CLAIMS

1.-59. (Canceled)

60. (Currently Amended) A semiconductor device comprising:

a substrate having a front surface and a rear surface;

a first insulating film comprising silicon oxide provided over said front surface of said substrate;

a second insulating film comprising aluminum nitride and oxygen provided over said first insulating film;

a third insulating film comprising oxide provided over said second insulating film;

a transistor provided over said third insulating film, said transistor having at least a channel formation region, a source region, a drain region, a gate insulating film adjacent to said channel formation region, and a gate electrode adjacent to said channel formation region with said gate insulating film interposed therebetween;

an interlayer insulating film comprising a leveled upper surface over said transistor; and

a pixel electrode over said interlayer insulating film,

wherein crystallinity of said source region or the drain region is higher than ~~crystalinity~~ crystallinity of said channel region.

61. (Currently Amended) A semiconductor device comprising:

a substrate comprising a front surface and a rear surface;

a first insulating film comprising silicon oxide provided over said front surface of said substrate;

a second insulating film comprising aluminum nitride and oxygen provided over said first insulating film;

a third insulating film comprising oxide provided over said second insulating film;

a transistor provided over said third insulating film, said transistor having at least a channel formation region, a source region, a drain region, a gate insulating film adjacent to said channel formation region, and a gate electrode adjacent to said channel formation region with said gate insulating film interposed therebetween;

an insulating film over said transistor; and

a pixel electrode over said insulating film,

wherein crystallinity of said source region or the drain region is higher than ~~crystalinity~~ crystallinity of said channel region.

62. (Previously Presented) The device of claim 60 wherein said substrate is a glass substrate.

63. (Previously Presented) The device of claim 61 wherein said substrate is a glass substrate.

64.-76. (Canceled)

77. (Currently Amended) A semiconductor device comprising:

a substrate;

a first insulating film comprising silicon oxide over said substrate;

a second insulating film comprising aluminum nitride and oxygen formed [[on]] over said first insulating film;

a third insulating film comprising oxide formed [[on]] over said second insulating film; and

a transistor provided over said third insulating film, said transistor having at least a channel formation region, a source region, a drain region, a gate insulating film adjacent to said channel formation region, and a gate electrode adjacent to said channel formation region with said gate insulating film interposed therebetween,

wherein crystallinity of said source region or the drain region is higher than ~~crystalinity~~ crystallinity of said channel region.

78. (Previously Presented) The semiconductor device according to claim 77, wherein said semiconductor device is an active matrix display device.

79. (Previously Presented) The semiconductor device according to claim 77, wherein said semiconductor device comprises a pixel portion and a driver portion over said substrate.

80.-88. (Canceled)

89. (Previously Presented) The semiconductor device according to claim 77,

wherein said transistor comprises:

a semiconductor film formed on said third insulating film, said semiconductor film comprising at least said channel formation region, said source region, and said drain region;

a gate insulating film formed on said semiconductor film; and

a gate electrode formed on said gate insulating film.

Rejoinder of Previously Withdrawn Claims 77-79 and 89

Claim 60 and 61 are allowable. Claims 77-79 and 89, previously withdrawn from consideration as a result of a restriction requirement, each after amendment include all the limitations of an allowable claim. Pursuant to the procedures set forth in MPEP § 821.04(a), **the restriction requirement among species with respect to these claims, as set forth in the Office action mailed on January 25, 2008, is hereby withdrawn** and claims 77-79 and 89 are hereby rejoined and fully examined for patentability under 37 CFR 1.104. In view of the withdrawal of the restriction requirement, applicant(s) are advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application. Once the restriction requirement is withdrawn, the provisions of 35 U.S.C. 121 are no longer applicable. See *In re Ziegler*, 443 F.2d 1211, 1215, 170 USPQ 129, 131-32 (CCPA 1971). See also MPEP § 804.01.

Claims 77-79 and 89 are rejoined.

Allowable Subject Matter

Claims 60-63, 77-79 and 89 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Friday, 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Shouxiang Hu/
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